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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,283	08/27/2003	Takayuki Kitazawa	031080	4445

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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,283	KITAZAWA ET AL.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-15 and 18-22* is/are pending in the application.

4a) Of the above claim(s) *16 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,3,7-15 and 18-22* is/are rejected.

7)☐ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's amendments and arguments, filed 11/06/2006, with respect to the rejections have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made below.

112 2nd traversal

Applicant's have amended claims 1 and 18 in response to previous action, and submit the amendments made overcome the previous 112 2nd paragraph rejections. The phrase pointed out in at least the last action (08/04/2006)

"a control bias supply circuit that supplies a control bias for cutting off all the switching transistors to the switching transistors"

Applicant's amendments made to claims 1 and 18 fail to address this cited limitation.

Applicant's response on (06/15/2006)

> "It is respectfully submitted that claims 1 and 18 particularly point out and distinctly claim the subject matter. More specifically, it is submitted that one of ordinary skill in the art would readily understand that claims 1 and 18 each call for a control bias supply circuit that supplies a control bias to the switching transistors, wherein the control bias cuts off all the switching transistors."

It is submitted the description of the operation of the control bias supply circuit by Applicant on (06/15/2006) clearly and definitely recites the operation of the control bias supply circuit, however this not the operation of the recited limitations of claim 1 and 18.

Nevertheless in effort to reduce the matters for the purposes of appeal the previous 112 2nd rejections have been withdrawn and in place made objections.

Claim Objections

Claim 1 recites the limitation "a control bias for cutting off all the switching transistors to the switching transistors when all of the switching transistors are in a non-selected state." It cannot be determined by the office what applicant intends by cutting off all of the switching transistors to the switching transistor.

Claim 18 recites a similar limitation "supplying a control bias for cutting off all the switching transistors to the switching transistors when all the switching transistors are in a non-selected state." Similarly it cannot be determined by the office what applicant intends by cutting off all of the switching transistors to the switching transistor.

Claim 11 recites the limitation "the input terminal...the output terminal" in lines 2 and 3. As Applicant has deleted the limitations, which provide the antecedent basis the claims no longer has proper antecedent basis for the claimed limitations.

Claim 14 recites the limitation "The switch circuit as claimed in claim 2", however Applicant has canceled claim 2 therefore there is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7, 10, 14, 18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Bialo (U.S. Pat. No. 4,719,374)

With respect to claims 1 and 18 Bialo teaches a switching circuit (Fig. 1 and detailed embodiment shown in Fig. 4) comprising: switching transistors (Fig. 1 FET15 and 16 or 58 and 60 in figure 4) commonly connected to a connection node (node 8) a control bias supply circuit (control circuitry best seen in figure 4 connected to gate terminals of the transistors 58 and 60) that supplies a control bias (bias voltage to bias FETs in cutoff) for cutting off all the switching transistors to the switching transistors (FETs 58 and 60) in order to prevent (col. 2 lines 7-15 and 49-60) high frequency signal from substantially propagating through all the switching transistors (FETs 58 and 60) when all of the switching transistors are in a non-selected state in which all the switching transistors are turned OFF in response to selection control signals applied thereto.

With respect to claim 7 Bialo teaches the control bias supply circuit varies a voltage value (from high to low to control the conduction of the FETs 11 and 12) of the control bias.

With respect to claim 14 Bialo teaches the common connection node is connected to a ground potential through a resistor (item 62 or 18).

With respect to claims 10 and 22 Bialo teaches supplying the control bias having a first voltage value (ON voltage) when at least one of the switching transistors is in a selected state and supplying the control bias having a second voltage (off voltage) value different from the first voltage value when all the switching transistors are in the non-selected state.

Alternatively Claims 1, 3, 7, 10-12,18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Kohama et al. (U.S. Pat. No. 5,731,607)

With respect to claims 1 and 18 Kohama teaches a switching circuit (Fig. 5) comprising: switching transistors (FET11 and 12) commonly connected to a connection node (node intersecting or between FETS 11, 12) a control bias supply circuit (CTL1) that supplies a control bias for cutting off all the switching transistors (FETs 11 and 12) to the switching transistors (FETs 11 and 12) in order to prevent (improve isolation col. 4 lines 40-45) high frequency signal (RF signal described in col. 1 as 1.9 and 1.66 GHz) from substantially propagating (propagating from RF1 to RF2) through all the switching transistors when all of the switching transistors are in a non-selected state in which all the switching transistors are turned OFF in response to selection control signals applied thereto.

With respect to claim 3 Kohama teaches the control bias supply circuit supplies the control bias in accordance with a voltage signal that is applied from outside of the switching circuit (i.e. not seen in switch circuit 11 in Fig. 5).

With respect to claim 7 Kohama teaches the control bias supply circuit varies a voltage value (from high to low to control the conduction of the FETs 11 and 12) of the control bias.

With respect to claim 11 Kohama teaches at least three switching transistors, which are commonly connected (See Fig. 5)

With respect to claim 12 Kohama teaches a shunt transistors (FET13) respectively provided for the switching transistors and are connected between the connection node and a given potential, gates of the shut transistors receiving the select control signals.

With respect to claims 10 and 22 Kohama teaches supplying the control bias having a first voltage value (ON voltage) when at least one of the switching transistors is in a selected state and supplying the control bias having a second voltage (off voltage) value different from the first voltage value when all the switching transistors are in the non-selected state.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bialo (U.S. Pat. No. 4,719,374)

With respect to claim 3 Bialo teaches the control bias supply circuit supplies the control bias in accordance with a voltage signal that is from control circuitry identified as control circuitry item 21 and 22. Bialo does refer to this section as outside the switching circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the input voltage signal used to be located outside of the switching circuit in order reduce the size of the switching circuit.

Claims 8-9, 13, 19 and 20-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Bialo (U.S. Pat. No. 4,719,374) in view of Matsunaga et al. (U.S. Pub. No. 20030016082)

With respect to claims 8-9 and 20-21 Bialo teaches the device of claim 1 as understood by the examiner, however Bialo does not teach the control bias varies the control voltage of the control bias circuitry when the switching circuits are in a non-selected states. Matsunaga teaches the use of a control bias circuit, which teaches the capability of varying the voltage, supplied the voltage control terminals of switching transistors. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Bialo to use a control bias circuit similar to that seen in Matsunaga in order to prevent excess current flow to the switching transistors.

With respect to claims 13 and19 Bialo teaches the device of claim 1. Bialo does not teach the use of MESFET in the control bias supply circuit. Matsunaga teaches the use of transistors in the bias control circuitry if it is held no transistors are to be connected to the control terminal of Bialo. Bialo teaches the use of FETs. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a MESFET over another type of FET to increase the switching speed

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bialo (U.S. Pat. No. 4,719,374) in view of Ayasli et al. (U.S. Pat. No. 5,012,123) Bialo does not teach the use of a shunt transistor connected to a source of a first one of the switching transistors, wherein a voltage signal applied to a gate of a second one of the switching transistors is applied to a gate of the shunt transistor. Ayasli teaches the use of a shunt resistor. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a shunt resistor reduce noise.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bialo (U.S. Pat. No. 4,719,374) in view of Ayasli et al. (U.S. Pat. No. 5,012,123) Bialo does not teach ballast resistors, each of which is connected between a source and a drain of a corresponding one of the switching transistors. Ayasli teaches the use of ballast resistors see fig 4. It would have been obvious to one of ordinary skill in the art at the time of the invention to in order to establish a biasing voltage source and drain of the switching transistor.

Allowable Subject Matter

Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 4 Bialo teaches the switching circuit of claim 1 however does not teach the control bias supply circuit comprises a diode having an anode to which the voltage signal is applied and a cathode via which the control bias is output to the connection node. At least this further limitation to claim 1 is not taught or rendered obvious by the prior art of record.

With respect to claims 5 and 6 Bialo teaches the switching circuit of claim 1 however does not teach control bias supply circuit comprises a bias transistor including a structure of a MESFET; and the MESFET having a gate receiving a voltage signal, a first terminal connected to a given potential via a capacitive element, and a second terminal connected to the connection node, the control bias being supplied to the connection node from the second terminal. At least this further limitation to claim 1 is not taught or rendered obvious by the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-

272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

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